RESPONSE

Claims 1-29 were pending in the Application. Claims 1–12 and 14–29 were rejected, and claim 13 was objected to. Applicant respectfully thanks the Examiner for suggesting that objected claim 13 would be allowable if rewritten in independent form. The Applicant believes that amended independent claims 1, 19, and 24 are now in allowable form. The Applicant respectfully submits that amended independent claims 1, 19, and 24 claims, as well as their dependent claims, are patentable over the cited references.

Claims Status

Claims 1–29 were pending in the Application. Claims 1–12 and 14–29 stand rejected and claim 13 stands objected to. Claim 14 is cancelled by the present Amendment.

Claims 1, 5, 19, 22, 24, and 28 are amended by the present Amendment to state that a "bus status" refers to a "bus idle status." Support is found for this amendment in paragraphs [0019] and [0039] of the specification and in claim 14 as originally filed.

Claims 1, 7-11, 13, 18, and 19 are amended by the present Amendment to clarify that a received isolation signal is received on "a device isolation control line." Support for this amendment is found throughout the specification. For example, in paragraph 0028, "[t]he isolation control logic 36 also includes error monitor and control logic 68 in communication with the device state registers 62, the bus error registers 64, the hot-plug logic 66, the bus interface logic 38, the IOVA error detector 44, and the protocol checker 46." All of these communicate with the isolation control logic over a device isolation control line. This is further illustrated in FIG. 4 where signal lines connect the ISOLATION CONTROL LOGIC to system software 42, the IOVA error detector 44, and the protocol checker 46. Further support may be found in paragraphs 0032 and 0038.

Claim 1 is also amended to state "[a]n apparatus for isolating, in response to a device isolation signal and a bus idle status signal..." Support may be found throughout the specification. For example, support for this amendment is found in paragraphs 0020 and 0037.

Claims 2-4, 6, 12, 15-17, 20-21, 23, 25-27, and claim 29 are presented as originally filed. Upon entry of the present Amendment and Response After Final, claims 1-13 and 15-29 will be pending and are presented for reconsideration.

Rejections Under 35 U.S.C. § 102

Claims 1-4 and 6-12 were rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,815,647 to Buckland et al. ("Buckland"). Claims 1, 2, 4, 5, 7–10, and 14-29 were rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 6,032,271 to Goodrum et al. ("Goodrum"). Applicant hereby restates and further clarifies the summaries provided in the Response dated April 21, 2004.

Buckland

Buckland "relates to computer systems having a central processing unit (CPU) and plural devices, or feature cards for performing specific system functions." Col. 1, lines 23-26. Buckland addresses the need "for a system that would allow a CPU to identify which specific device on a particular adapter card generated an error signal." Col. 1, lines 62-64. Buckland further discloses error recovery techniques. Abstract.

Specifically, Buckland teaches "a computer system having additional control logic . . . provided with a bridge chip and at least one connector slot for receiving a feature card, that implements specific functions such as I/O, memory, or the like." Col. 2, lines 23-26. "This chip provides the interface between the I/O bus and the actual adapter slot 106 which includes a connector 4 and additional logic." Col. 6, lines 12-15.

Buckland includes a schematic diagram illustrating the signals required for I/O adapter slots to be isolated. Col. 2, line 66, through col. 3, line 2, and Figure 9. Buckland also includes a flow chart that includes isolation in the error recovery. Col. 3, lines 3-4, and Figure 10. As Buckland's Figure 9 shows, "[t]he I/O bus 102 . . . is connected to a bridge chip 104, and in combination with the additional control logic 105, is used to control a single PCI slot 106." Col. 6, lines 48-50. "One modified bridge chip 104 in conjunction with one set of control logic 105 is used to control one slot 106." Col. 6, lines 56-58.

Buckland holds a device in a reset state in response to an error signal associated with the device. Figure 10. As Buckland explains with respect to Figure 10:

> [If a system error signal] SERR# signal is present from one of the plurality of devices on the adapter cards in the computer system . . . , the reset signal RST# is activated (by bridge chip 104) to the device signaling SERR#, to place the device 5 in its reset state and avoid any damage to the system, while still keeping the device coupled to the system. That is, the slot 106 having the feature card which issued the SERR# signal is reset in the manner previously described (data processing activity is ceased). At step 5, the status bit in register 203 is set, e.g. to logical 1. Next, at step 6, the control hardware as shown in FIG. 9 will ignore all load and store operation, and abort any pending direct memory access (DMA) operations. . . . If there are no additional load/store operations, then at step 8 the device driver reads the status bit in register 203 of bridge chip 104. . . . However, if at step 5 the status bit was set to indicate the presence of an SERR# signal, then bridge chip 104 is reconfigured (by re-initialization) at step 11. Typically the device driver will reset the feature card by re-initializing the device. . . . Thus, it can be seen how the present invention allows a computer system to isolate a single device in a particular I/O slot 106 . . . .

Col. 12, line 61, through col. 13, line 42 (emphasis added). In summary, Buckland generates a device isolation signal in response to a ***device*** status signal. Namely, a system error signal (SERR#) is generated by the device and in response, a bridge chip generates a device reset signal (RST#).

Goodrum

Goodrum "relates to fault isolation." Col. 1, line 7. Generally, Goodrum "features a computer system having devices, mass storage accessible by at least one of the devices, and a watcher for monitoring for a faulty condition." Col. 1, lines 21-24. Goodrum teaches that "[t]he devices are coupled to a bus, and the faulty condition includes a bus hang condition." Col. 1, lines 38-40. "The watcher includes a bus timer to monitor the bus to detect the bus hang condition." Col. 1, lines 40-41. "The bus hang condition is present if the bus timer expires." Col. 1, lines 41-42. Further, Goodrum teaches that a "fault isolation controller is used to turn off all the devices when the bus hang condition is detected and to turn the devices back on to test the devices." Col. 1, lines 42-45. "The faulty device is identified if the bus hang condition occurs when that device is tested." Col. 1, lines 46-48.

Specifically regarding fault isolation, Goodrum explains:

> The bus watcher 129 can detect for a hang condition on the secondary PCI bus 32. If a hang condition is detected, the bus watcher 129 sets a bus hang pending bit, which causes the SIO 50 to power down to slots on the secondary PCI bus 32 and a non-maskable interrupt (NMI) to be transmitted to the CPU 14. The CPU 14 responds to the NMI by invoking an NMI routine to isolate the slot(s) causing the hang condition. Once identified, the defective slot(s) are disabled or powered off.

Col. 86, lines 56-64. Goodrum describes the second part of the process in more detail with respect to Figure 37:

> Referring to FIG. 37, the NMI handler first determines 400 if the bus hang pending bit is set by reading the bus hang indication register 482. If so, the NMI handler calls 401 a BIOS isolation handler for isolating the defective slot or slots. Otherwise, other NMI procedures are called 402.

Col. 87, lines 59-64. In Goodrum, a device is isolated in response to the detection of a bus hang condition. Figure 37. Goodrum also defines examples of bus hang conditions detected by the watch-dog timer:

> "The following are examples of bus-hang condition that can be detected by the watch-dog timer 454: The FRAME__ signal is stuck high or low; the signal TRDY__ is not asserted in response to IRDY__; the PCI arbiter 124 does not grant the bus to any master; and a master requesting the bus 32 keeps getting retired."

Col. 87, lines 44-49. Additionally:

> "... the invention features a computer system having a bus, a watcher for detecting an illegal condition on the bus... The illegal condition occurs when a PCI signal TRDY__, STOP__, or DEVSEL___ is asserted during a bus idle condition."

Col. 2, lines 33-35.

In Goodrum, the watcher includes a bus timer to monitor for the bus hang condition. Detection of the bus hang condition sets a bus hang pending bit. The bus hang pending bit being set, in turn, causes the fault isolation controller to turn off all the devices potentially causing the bus hang condition. Col. 1, lines 40-44; Col. 87, lines 50-55. The bus hang condition, or "illegal condition," as defined by Goodrum, may "occur when a PCI signal TRDY__, STOP__, or

DEVSEL___ is asserted during a bus idle condition," or when "the FRAME___ signal is stuck high or low..." Col. 2, lines 33-35; Col. 87, lines 44-49.

Rejection of Independent Claim 1 Under § 102 Over Buckland

The Office Action of June 30, 2004 suggests that Buckland anticipates all of the elements of original claim 1. As amended, independent claim 1 recites, in part, "bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the idle status of the bus."

Applicant respectfully submits that independent claim 1 is patentable over Buckland as amended. As the Examiner has pointed out, Buckland teaches in Col. 12, lines 24-48, "the device driver 201 has the responsibility for checking the status of the device itself or to make sure that the operation is completed correctly at specific points in the code." Buckland, however, continues with, "[r]egister 203 will contain some bit where, e.g. a logical 0 will indicate that there is no error present and the device driver can read the information from the I/O device. However, if the status bit in register 203 contains a logical 1 and the bridge chip 104 is holding device 5 in the reset state (RST# active), then when the device driver reads the information from the device all the bits will be set to logical ones, thus, indicating to the driver that the operation did not complete properly" (emphasis added).

Amended claim 1, interpreted in light of the supporting specification, refers to the idle status of the bus, not of the device. In paragraph 0019 of the specification, the Applicant states, "[t]he bus interface logic 38 monitors the status of one or more of the signals of the bus 12 and generates a bus status signal (STATUS) indicating the status of the signal activity of the bus, e.g., idle or busy" (emphasis added). Further, originally filed claim 14 states, in part, "wherein the bus status signal is an idle status signal." Buckland teaches reading from the device registers, or a combination of the device registers and the device state, i.e., a reset (RST#). Respectfully, the Applicant submits that the present invention does not practice Buckland because the present invention generates a bus idle status signal, e.g., if the bus is "idle or busy", not a device control signal, i.e., a reset state. Further support for this may be found in the specification in paragraph 0019 where the Applicant states, "[i]n one embodiment, the bus interface logic 38 monitors the operational state of the bus 12 and generates the STATUS signal indicating the state of the bus

12. For example, in a PCI bus, the bus interface logic 38 may monitor the IRDY#, TRDY# and FRAME# signals." In light of the specification, the bus interface logic monitors device status signals, e.g., IRDY#, TRDY# and FRAME# and then generates a new bus STATUS signal based upon the status of the bus, e.g., idle or busy. The preceding signals are specified in Applicant's specification as examples, but they belong to the same class of signals as RST#; that is, device signals. Therefore, Buckland does not teach "bus interface logic in communication with the bus, the bus interface logic *generating a signal indicating the idle status of the bus.*"

Amended independent claim 1 also stands rejected over Buckland, the Office Action citing Buckland's teaching in Col. 6, lines 45-63, that "each slot can be selectively reset with a RST# signal and power removed from the slot when an I/O card is to be removed, replaced, or installed." Respectfully, the Applicant submits that Buckland does not teach independent claim 1 as amended. Claim 1 recites in part "wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus idle status signal from the bus interface logic and the received device isolation signal on the device isolation control line."

The Office Action states, on page 3, "[f]urther, in column 6, lines 45-63, Buckland et al. discloses that each slot can be selectively rest [sic] with a RST# signal as indicated by a user and power removed from the slot when an I/O card is to be removed, replaced, or installed (a received isolation signal)." As described above, a bus idle status signal indicates the status of the activity on the bus, e.g., idle or busy, not the control of a device as is taught by Buckland, i.e., a reset signal (RST#). The Examiner cites Buckland's teaching of power removal to be the received device isolation signal. The removal of power from a slot is not "a received device isolation signal from [a] device isolation control line." "Power removed from the slot," is the absence of a signal, i.e., an electrical signal. A card may not receive a signal, isolation or otherwise, if it is not powered. Even if this were true, which the Applicant does not concede, Buckland does not also teach the use of a bus idle status signal. Therefore, Applicant respectfully submits that Buckland does not teach or suggest amended independent claim 1 as it does not teach the use of two signals, i.e., "transmit[ting] a switch isolation control signal in response to the generated bus idle status signal and a received device isolation signal from the device isolation control line."

Rejection of Independent Claim 1 Under § 102 Over Goodrum

The Examiner also rejected independent claim 1 over Goodrum in light of Col. 1, lines 28-45 (combining citations from separate remarks) and Col. 2, lines 33-47. Applicant respectfully submits that amended independent claim 1 is patentable over Goodrum.

As stated earlier, amended claim 1 recites in part, "bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the idle status of the bus" and "isolation control logic in communication with the bus interface logic, the device isolation control line, and the isolation switch, wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus idle status signal and the received device isolation signal on the device isolation control line."

As the Examiner notes, Goodrum teaches that a fault isolation controller is used to turn devices off by powering them off. Col 1, lines 37-45. The devices are coupled to a bus and the faulty condition includes a bus hang. Goodrum provides "examples of [a] bus-hang condition that can be detected by the watch-dog timer 454: The FRAME__ signal is stuck high or low; the signal TRDY__ is not asserted in response to IRDY__; the PCI arbiter 124 does not grant the bus to any master; and a master requesting the bus 32 keeps getting retired." Col. 87, lines 44-49. As stated with regard to the RST# signal in reference to Buckland, IRDY__, and TRDY__ are device statuses, not bus statuses, as bus status is defined in the Applicant's specification in paragraphs 0006 and 0019: "e.g., idle or busy" and original claim 14: "wherein the bus status signal is a bus idle signal." The "bus hang" that Goodrum teaches is deduced by the watch-dog timer from conflicting, or incorrect device statuses. A device that does not assert a TRDY__ signal in response to an IRDY__ within a given time period may indicate that the target device has a problem. This however is not a reflection on whether the bus is idle or busy as is disclosed in the Applicant's specification in paragraph 0019 or as stated in amended claim 1 (i.e., "bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the idle status of the bus"). Though Goodrum states that the hang condition is tested for during the bus's idle state, the illegal condition, e.g., the assertion of TRDY__ on an idle bus, is generated in response to the bus status. Therefore, Goodrum's device isolation signal is generated in response to the bus status, i.e., a hang status, not processed in tandem as is done in

the Applicant's invention. In light of foregoing, Applicant respectfully submits that Goodrum does not teach the elements of amended claim 1.

As put forth in the Response dated April 21, 2004, Applicant respectfully submits that Goodrum utilizes one signal, the illegal condition generated in response to the bus status, but Goodrum does not teach or suggest examining both the bus idle state and the device isolation signal. For clarification's sake, Goodrum teaches a serial test condition, i.e. "if idle, test for bus hang. If bus is hung, send isolation control signal", whereas Application, performs a parallel comparison, i.e., "if bus is idle and an isolation signal is received, send isolation switch control signal." Goodrum discloses a bus that is hung without being idle, e.g, "the FRAME# signal is stuck high or low," thereby teaching that an isolation signal may be generated when the bus is not idle. Col. 87, line 46. Therefore the bus status, e.g., idle or busy, is irrelevant to Goodrum's isolation switch control signal. Applicant however relies on both the idle status of the bus and the received isolation signal to generate an isolation switch control signal.

Further, the Examiner cites Goodrum as teaching that the illegal condition is a device isolation signal. Though the illegal condition occurs when a PCI signal TRDY__, STOP__, or DEVSEL__, is asserted during a bus idle condition, the illegal condition is not a device isolation signal received on a device isolation control line, i.e., it is not a signal instructing the system to isolate a device on the bus. Instead, the illegal condition is an input to the watcher. Col. 2, lines 33-37. The watcher then, in response, generates the device isolation switch control signal, defined by Goodrum as powering down the device. Col. 1, line 26-28. As state previously, Goodrum relies on one signal, the received device isolation signal, whereas the Applicant relies on the bus status signal and the received device isolation signal from the device isolation control line.

Neither Buckland nor Goodrum, alone or in combination, teach or suggest "bus interface logic in communication with the bus, the bus interface logic generating a signal indicating the idle status of the bus," and "isolation control logic in communication with the bus interface logic, the device isolation control line, and the isolation switch, wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated

bus idle status signal and the received device isolation signal on the device isolation control line," as recited in amended independent claim 1.

Therefore, in light of the current amendments, and because neither Buckland nor Goodrum teach or suggest, alone or in combination, an apparatus with "isolation control logic in communication with the bus interface logic, the device isolation control line, and the isolation switch, wherein the isolation control logic transmits an isolation switch control signal to the isolation switch in response to the generated bus idle status signal and the received device isolation signal on the device isolation control line," amended claim 1 is patentable over the aforementioned patents. Dependent claims 2-13 and 15-18 are patentable because they depend on a patentable base claim. These claims may also include other features not taught or suggested by the cited references.

Rejection of Independent Claim 19 Under § 102 Over Buckland and Goodrum

Amended independent claim 19 recites, in part, "In a system having a bus controlled by a bus controller, a device isolation control line, and having at least one bus device in communication with the bus via an isolation switch" and "receiving a signal on the device isolation control line identifying a bus device to be isolated, the bus device performing a bus transaction; receiving a bus idle status signal; and transmitting an isolation switch control signal responsive to both the received device isolation signal and the received bus idle status signal."

As described above, neither Buckland nor Goodrum, alone or in combination, teach or suggest a system with a device isolation control line that utilizes two signals, a bus status signal "e.g., idle or busy," and a received device isolation signal. Therefore, in light of the current amendments, and because neither Buckland nor Goodrum teach or suggest, alone or in combination, a system that "[receives] a signal on the device isolation control line identifying a bus device to be isolated, the bus device performing a bus transaction; [receives] a bus idle status signal; and [transmits] an isolation switch control signal responsive to both the received device isolation signal and the received bus idle status signal," claim 19 is patentable over the aforementioned patents. Dependent claims 20-23 are patentable because they depend on a patentable base claim. These claims may also include other features not taught or suggested by the cited references.

Rejection of Independent Claim 24 Under § 102 Over Buckland and Goodrum

Amended independent claim 24 recites, in part, "means for transmitting an isolation switch control signal responsive to both the received bus device isolation signal and the received bus idle status signal."

As described above, neither Buckland nor Goodrum, alone or in combination, teach or suggest utilizing two signals, a bus idle status signal "e.g., idle or busy," and a received device isolation signal as means for transmitting an isolation switch control signal. Therefore, in light of the current amendments, and because neither Buckland nor Goodrum teach or suggest, alone or in combination, an apparatus with "means for transmitting an isolation switch control signal responsive to both the received device isolation signal and the received bus idle status signal," claim 24 is patentable over the aforementioned patents. Dependent claims 25-29 are patentable because they depend on a patentable base claim. These claims may also include other features not taught or suggested by the cited references.

CONCLUSION

The Applicant respectfully thanks the Examiner for speaking with the Applicant's attorney on September 15, 2004. The Applicant also respectfully requests that the Examiner reconsider the application and claims in light of the foregoing Amendment and Response After Final, and respectfully submits that the claims are in condition for allowance. If, in the Examiner's opinion, a second telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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